PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: "ELECTRONIC DELAY ELEMENT"

Appellants: David Jia Chen et al.

Attorney Docket No.: ROC920030233US1

Serial No.:	10/665,654	**Examiner:**	Ryan C. Jager
Filed:	September 18, 2003	**Art Unit:**	2816

Board of Patent Appeals and Interferences
Commissioner for Patents
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APPELLANT'S REPLY BRIEF

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Sir:

In response to the Examiner's Answer dated November 20, 2007, the two month due date for response to which is January 22, 2008 (the first business day after January 20, 2008), Appellant hereby respectfully submits his reply brief in support of his appeal to the Board of Patent Appeals and Interferences of the Examiner's final rejection of claims 1-14 of the above-referenced application.

RESPONSE TO EXAMINER'S ARGUMENTS

THE INDEPENDENT CLAIMS ARE PATENTABLE OVER TAYLOR

The Examiner has taken the position that claims 1-14 are anticipated by Sato et al, U.S. Patent No. 5,602,798. In response, Appellant respectfully traverses this rejection, and submits that Sato does not disclose all the elements and limitations of the claimed invention. Consequently, the claims on file are not anticipated by Sato, and the allowance of these claims is earnestly solicited.

With reference to "uniform channel length transistors" as recited in independent claims 1 and 9-11

> "...wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;
>
> wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;..."

The Examiner points to "same structure" in col. 14, lines 35-36 and "same size" in col. 14, lines 65-66 of Sato. In other words, the Examiner is asserting that Sato's teaching of "same structure" is the same as "uniform channel length transistors" as recited for the presently claimed invention. Appellant respectfully disagrees with the Examiner's assertion.

Sato, at col. 14, lines 35-41 teaches:

> Gate circuits 60a-60n have the same structure, and each includes a plurality of (three) p-channel MOS transistors p1-p3 connected in series between the power supply node (Vcc) and an output node OD1, and also includes a plurality of (three) n-channel MOS transistors n1-n3 connected in series between output node OD1 and the ground node.

Sato, at col. 14, lines 61-67 teaches:

> As compared to a case of using a simple CMOS inverter formed of one p-channel MOS transistor and one n-channel MOS transistor, the number of gates connected in

> tandem can be reduced (provided that the transistors used therein have the same size), and an area occupied by the delay elements can be reduced.

As stated previously in the Appeal Brief, the term "same structure" has more than one connotation, i.e., each of the gate circuits 60a-60n have the same number of transistors, the same layout of transistors, the same type of transistors, and more. Appellant suggests that Sato is referring to the actual configuration of components of a gate when Sato states "same structure". Sato consistently uses the phrase "same structure" when referring to the composition of a circuit. For example, Sato at col. 6, lines 63-64 states (emphasis added):

> FIG. 4 is specifically shows a structure of the input circuit shown in FIG. 1

Sato at col. 8, lines 27-28 states (emphasis added):

> In particular, if all the input circuits have the same common structure as shown in FIG. 4…

Sato states under the "Brief Description Of The Drawings" that FIGs. 1, 4, 7, and 10-14 that a structure is shown for the respective device, signal, or circuit.

Sato at col. 10, lines 21-23 states (emphasis added):

> Input circuits 40c-40h have the same structure, and each include an inverter IV receiving an external signal through a corresponding terminal and 2-input NAND circuit NA receiving at one input the output signal of inverter IV.

Sato, at col. 10, lines 53-57, further states (emphasis added):

> However, according to the structure shown in FIG. 1, internal circuit 50g should be responsive not to the internal clock signal but to address status signal ADSN from internal circuit 50b operating in synchronization with the internal clock signal INT.CLK.

Sato, at col. 10, line 66 to col. 11, lines 1-5, further states (emphasis added):

> All internal circuits 40c-40h have the same structure. In FIG. 7, when internal snooze mode signal ZZ1 or ZZ2 designates the snooze mode, the output signal generated from each input circuit is set to the inactive state of high level. Input circuits 40b-40h may have another structure, in which case logic of signals is appropriately adjusted in internal circuits 50b-50g.

Sato, at col. 13, lines 14-15, further states (emphasis added):

> FIG. 10 specifically shows a structure of the internal snooze mode signal generating portion

Sato, at col. 13, lines 43-46, further states (emphasis added):

> FIG. 11 shows a specific structure of first delay element 45aa shown in FIG. 10. In FIG. 11, first delay element 45aa includes even stages of (eight in FIG. 11) cascaded CMOS inverters 56a-56h.

Sato, at col. 14, lines 8-23, further states (emphasis added):

> Each of capacitors 57a-57d may have a structure of a parallel electrode type, … Delay element 45ba has the same structure as that shown in FIG. 12. However, capacitors 57a-57d of the delay element 45ba have a small capacitance.

Sato, at col. 14, lines 24-27, further states (emphasis added):

> FIG. 13 shows a second modification of a structure of first delay element 45aa shown in FIG. 10. The structure shown in FIG. 13 additionally includes at the output portions of inverters 56i and 56j with resistance elements 58a and 58b.

Sato, at col. 14, lines 32-35, further states (emphasis added):

> FIG. 14A, shows a modification of a structure of the first delay element shown in FIG. 10. In FIG. 14A, first delay element 45aa includes even stages of (14 in FIG. 14A) cascaded gate circuits 60a-60n.

Sato, at col. 15, lines 1-2, further states (emphasis added):

> FIG. 14B shows a specific structure of second delay element 45ba shown in FIG. 10

As can be seen from the above cited portions of Sato, Sato is using the term "structure" to refer to the actual composition of components within a circuit. The presently claimed invention, on the other hand, states:

> "…wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;
>
> wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;…"

Sato teaches that gates have the same structure, which means that the gates comprise the same components, as can be seen from the above discussion. The presently claimed invention recites that the "...delay stages includes a stack of uniform channel length transistors..." Two or more gates comprising the same components is **not** the same as delay stages including a stack of uniform channel length transistors. The Examiner further supports the rejection of the independent claims by stating that Sato's teaching of "same size" in (emphasis added):

> As compared to a case of using a simple CMOS inverter formed of one p-channel MOS transistor and one n-channel MOS transistor, the number of gates connected in tandem can be reduced (provided that the transistors used therein have the same size), and an area occupied by the delay elements can be reduced.

is also evidence that Sato teaches uniform channel length transistors.

However, Appellant respectfully disagrees. Sato never teaches what is meant by "size". The term "size" also has more than one connotation. For example, "size" can refer to the physical size of the transistor, the width of the transistor channel, the length of the transistor channel, the capacitance of the transistor, and a multitude of other things. Even though the Examiner cites three new U.S. Patents 4,431,973; 5,724,108; and 5,952,854 that state "same size" refers to the same channel length and channel width, Sato does not explicitly teach this. See Book entitled Computers by Sajjan G. Shiva - 1998 ISBN 0824700821 available at online URL (www.books.google.com) where "*Transistor size is determined by the channel width (W) and length (L).*" Therefore, Sato at most teaches "size" without more specificity, whereas the present invention recites only uniform channel length.

Furthermore, the presently claimed invention further recites that the inclusion of uniform channel length transistors is "without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip" and "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Sato is completely silent on these additional claim elements.

The Examiner states that because Sato teaches "same structure" and "same size", that Sato therefore teaches "… so that tolerances across the delay stages track tolerance of other circuits on a chip" and "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". However, Appellant respectfully disagrees. Sato is completely silent on "… so that tolerances across the delay stages track tolerance of other circuits on a chip" and "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Sato is only concerned with circuits only in the delay elements. The presently claimed invention, on the other hand, is directed towards a delay element that does not use extended channel length transistors, but includes uniform channel length transistors, so that so that "that tolerances across the delay stages track tolerance of other circuits on a chip".

The use of uniform channel length transistors allow for the tolerances across the delay stages to track other circuits on the chip and not just the delay element. Appellants respectfully suggest that the Examiner is improperly interpreting the claim to recite that uniform channel length transistors are included in a delay stage so that tolerances can be track only across delay stages in a delay element and not "across other circuits in the chip". Sato never teaches tracking tolerances. Even assuming arguendo that "same structure" in Sato is analogous to uniform channel length transistors, which it is not, Sato never teaches that the "same structure" allows for having tolerances for gate circuits in the delay stage track other tolerances across other circuits (e.g. other circuits besides that particular delay element) on the chip. Sato is only concerned with a single delay element and the gate circuits within that delay element.

Moreover, nowhere does Sato teach or suggest "the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Sato is directed towards the post-production stage of the circuit and is not concerned with providing uniform tolerance variations a circuit across a circuit during production. A post-production stage such as manufacturing/yield is not the same as parametric tracking. Yield is one measurement among several of the efficiency in a

chip manufacturing process. Manufacturing yield is a reflection of the quality of the manufacturing process and drives cost. The presently claimed invention, on the other hand, is concerned with the manufacturing process, which naturally varies from wafer to wafer, by using parametric tracking. Designs that use a mixture of channel lengths result in non-uniform tolerance variations across the chip.

Additionally, the Examiner states that because "Sato is completely silent on using extended channel length transistors; therefore it is evident that his delay circuit is configured without using extended channel length transistor (*Sic*)". Appellants suggest that it is evident that the delay circuit in Sato is configured without using extended channel length transistors, then the Examiner should be able to point to a location in Sato, where Sato teaches this. However, Sato does not teach this claim element as even noted by the Examiner ("Sato is completely silent on using extended channel length transistors").

The Examiner cites 35 U.S.C. § 102(b) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims as being anticipated by Sato.[1] Because the elements in independent claims 1 and 9-11 are not taught or disclosed by Sato, the presently claimed invention distinguishes over Sato for at least this reason.

As discussed above, the independent claims are patentable over the Sato reference. Since dependent claims contain all the limitations of the independent claims, claims 2-8 are patentable over Sato as well.

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[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of Californi*a, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application and all of the pending claims are in condition for allowance. Reversal of the final rejection of claims 1-14 is respectfully requested.

Respectfully submitted,

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